



AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): ~~an~~ An electronic control unit comprising:
a first control circuit section containing a program memory, an operation processing RAM memory, a microprocessor, and a first series-parallel converter; and
a second control circuit section containing a communication control circuit section at least for carrying out communication of monitoring and control signals, a data memory, and a second series-parallel converter; ~~and,~~
~~in which~~ wherein serial communication of monitoring and control signals is carried out mutually between said first and second control circuit sections via said first and second series-parallel converters;
wherein said first control circuit section includes regular transmission means and irregular transmission means, and said second control circuit section includes regular report means and an unprocessed data table;
wherein said regular transmission means acts as write setting means that regularly transmits a control output data or a constant set data from said first control circuit section with respect to said second control circuit section, and executes a retransmission processing from the first control circuit section to the second control circuit section ~~in the case of if presence of any~~

communication error in a confirmation reply of whether or not the second control circuit section has received said regular transmission data, is present;

wherein said regular report means acts as one-way input readout means which regularly reports ~~a~~-monitoring input data and status information from said second control circuit section to said first control circuit section, whereby no confirmation reply of whether or not the first control circuit section has received said regular report data is carried out;

wherein said irregular transmission means ~~acts~~-operates as transmission means that is applicable when any error is present in a report communication provided by said regular report means, and is ~~also applied when required as to~~ applied if a readout request for ~~a~~-monitoring input data of a specified address from said first control circuit section to said second control circuit section is required, and if a readout request for reading out and checking a write save data having been written and set by said regular transmission means is required;

wherein said irregular transmission means further ~~acts~~-operates as readout request means that makes a readout request ~~again~~ from the first control circuit section to the second control circuit section ~~in the case of presence of~~ if any communication error in a report reply of a monitoring input data of a specified address or a write save data is present, said report reply being carried out as a confirmation reply ~~to the fact that~~ related to said second control circuit section ~~has~~-having received said irregular transmission data;

wherein said unprocessed data table ~~acts~~-operates as a receiving-side command memory arranged so as to sequentially save ~~a~~-command data for executing a confirmation reply when said second control circuit section receives any transmission data from said first control circuit

section, and to sequentially erase said saved data when said second control circuit section transmits the confirmation reply data to said first control circuit section; and the transmission of a regular report data ~~can be~~ is carried out while preventing upstream communication jam-up from said second control circuit section to said first control circuit section with said unprocessed data table.

2. (currently amended): The electronic control unit according to claim 1, wherein said first control circuit section comprises a reply-waiting data table and retransmission means; wherein said reply-waiting data table ~~acts~~ operates as a transmission-side command memory arranged so as to sequentially save a transmission command that said first control circuit section has transmitted to said second control circuit section with regular transmission means and irregular transmission means, and to sequentially erase said saved command when receiving a confirmation reply data or a report reply data from the second control circuit section; ~~and,~~ wherein said retransmission means ~~acts as means that~~ operates when there is any communication error in a confirmation reply or a report reply to said regular transmission means or irregular transmission means, or when a leading transmission command having been stored in said transmission-side command memory is not erased even after a predetermined time period has passed, and transmits ~~again a~~ transmission data based on said error transmission command; and

wherein a transmission command having been transmitted again is deleted from and re-stored in said transmission-side command memory, and a first-in first-out processing is carried out.

3. (currently amended): The electronic control unit according to claim 1, wherein said second control circuit section comprises readout request setting means;

wherein said readout request setting means ~~acts-operates~~ as means for making the request for the readout of a selected data memory of a specified address that is provided in said second control circuit section by adding a readout request flag to a status information contained in said regular report means; and

wherein said first control circuit section is arranged so as to ~~operates-operate~~ when there is a communication error in said regular report data, or when said readout request is present, and ~~to be capable of making~~ is operable to make a readout request for a regular report content or a selected data memory with said irregular transmission means.

4. (currently amended): The electronic control unit according to claim 1, wherein at least one of said regular transmission means or regular report means comprises division circulating means; and

wherein said division circulating means ~~acts-operates~~ as means that divides a large number of control output data intended to be regularly transmitted or a large number of monitoring input data intended to be regularly reported, and sequentially divides and transmits or

sequentially divides and reports in a cycle corresponding to a required emergency degree, whereby a data amount to be transmitted or reported at a single communication is suppressed.

5. (currently amended): The electronic control unit according to claim 1, wherein said first control circuit section comprises regular report permission means; and

| said regular report permission means ~~aets-operates~~ as means for storing a command data that is transmitted by said regular transmission means to a memory of a predetermined address provided in said second control circuit section, and ~~aets-operates~~ to permit the second control circuit section to transmit said regular report.

6. (currently amended): An electronic control unit comprising:
a first control circuit section containing a program memory, an operation processing RAM memory, a microprocessor, and a first series-parallel converter; and a second control circuit section containing a communication control circuit section at least for carrying out communication of monitoring and control signals, a data memory, and a second series-parallel converter; and,

| ~~in which~~ wherein serial communication of monitoring and control signals is carried out mutually between said first and second control circuit sections via said first and second series-parallel converters;

wherein said first control circuit section includes regular transmission means and irregular transmission means, and said second control circuit section includes regular report

means; said first and second control circuits section include first and second communication error determination means, first and second adding-subtracting means, and first and second error occurrence definition means respectively, and said first control circuit section includes

retransmission means;

wherein said regular transmission means ~~aets-operates~~ as write setting means that regularly transmits ~~a-control~~ output data or ~~a-constant~~ set data from said first control circuit section to said second control circuit section, and executes retransmission processing from the first control circuit section to the second control circuit section ~~in the case of presence of~~ if any communication error in confirmation reply of whether or not the second control circuit section has received said regular transmission data; is present,

wherein said regular report means ~~aets-operates~~ as one-way input readout means which regularly reports ~~a-monitoring~~ input data and status information from said second control circuit section to said first control circuit section, whereby no confirmation reply of whether or not the first control circuit section has received said regular report data is carried out;

wherein said irregular transmission means ~~aets-operates~~ as transmission means that is applicable when any error is present in a report communication provided by said regular report means, and is ~~also applied when required as to~~ applied if a readout request for ~~a-monitoring~~ input data of a specified address from said first control circuit section to said second control circuit section is required, and if a readout request for reading out and checking a write save data having been written and set by the mentioned regular transmission means; is required,

wherein said irregular transmission means ~~aet-operates~~ as readout request means that makes a readout request ~~again~~ from the first control circuit section to the second control circuit section ~~in the case of presence of~~ if any communication error in a report reply of a monitoring input data of a specified address or a write save data is present, said report reply being carried out as a confirmation reply to ~~the fact that~~ said second control circuit section ~~has~~ having received said irregular transmission data;

wherein said first and second communication error determination means ~~aet-operate~~ as plural types of receiving error determination means that determine presence ~~of~~ or absence of any error regarding various regular and irregular communication packets that a control circuit section on the side where the mentioned determination means is provided has received from the other control circuit section, or that ~~discriminate~~ determine a state that any communication packet to be received cannot be received;

wherein said first and second adding-subtracting means ~~aet-operate~~ as operation means that adds or subtracts a second variation value when any of said plural types of receiving error determination means determines the presence of error, and subtracts or adds a first variation value when all the receiving error determination means determine the absence of any error to perform an addition-subtraction compensation with respect to a current value memory so as to offset each other, and stops an addition-subtraction compensation with said first variation value at a predetermined normal-side limit value when the determination of the absence of error continues;

wherein said first and second error occurrence definition means ~~aet-operate~~ as comparison means that ~~generates-generate~~ first and second error detection signals when a current value of said adding-subtracting means gets out of a scope of a predetermined abnormal-side limit value as a result of accumulation of said first and second variation values;

wherein said retransmission means ~~is means, which operates-operate~~ when any error is present in a transmission data provided from said first control circuit section to the mentioned second control circuit section, or when error is present in a confirmation reply data in response to said transmission data, and with which the first control circuit section transmits ~~again-a~~ communication packet corresponding to the old transmission command, and adds or subtracts a second variation value with respect said first adding-subtracting means; and

wherein said second variation value is set to a value smaller than a permitted accumulation value, being a difference between said abnormal-side limit value and normal-side limit value, and stopping the operation, or initialization and restart of said first or second control circuit section is carried out responsive to the occurrence of said error detection signal.

7. (currently amended): The electronic control unit according to claim 6, wherein said first and second control circuit sections comprise first and second initialization means;

wherein said first initialization means ~~aets-operates~~ as means that operates when said first error occurrence definition means generates an error detection signal, resets a current value of said first adding-subtracting means at a predetermined initialization value at the start of

operation, and initializes and restarts a communication control circuit section provided in said second control circuit section;

wherein said second initialization means ~~aets-operates~~ as means that operates when said second error occurrence definition means generates an error detection signal, resets a current value of said second adding-subtracting means at a predetermined initialization value at the start of operation, and initializes to restart or stop the operation of a microprocessor provided in said first control circuit section; and

wherein an initialization value of the first and second adding-subtracting means to be reset by said first and second initialization means is a value close to said abnormal-side limit value from said normal-side limit value.

8. (currently amended): The electronic control unit according to claim 6 , wherein said first and second communication error determination means comprise at least one of bit information monitoring means and reply delay monitoring means or receiving interval monitoring means;

wherein said bit information monitoring means ~~aets-operates~~ as bit error determination means for determining presence or absence of any lack or mix in bit information such as parity check or sum check relative to a serial data communicated between said first and second control circuit sections;

wherein said reply delay monitoring means acts as reply response error determination means for making an error determination at the first control circuit section, being a source side

when a reply data from said second control circuit section in response to any data, which said first control circuit section has transmitted, cannot be received even when a predetermined reply response time period has passed;

wherein said receiving interval monitoring means ~~acts~~operates as receiving interval error determination means for making an error determination when a receiving interval time period of the other-side control circuit section with respect to a regular transmission data that said first control circuit section transmits or a regular report data that said second control circuit section transmits exceeds a predetermined value; and

wherein said adding-subtracting means performs an addition-subtraction compensation with a first variation value when none of said bit information monitoring means, reply delay monitoring means, and receiving interval monitoring means makes an error determination.

9. (currently amended): The electronic control unit according to 8, wherein said second variation value, which said adding-subtracting means adds or subtracts when the determination of said bit information monitoring means is a communication error, is a value larger than said first variation value; and wherein a variation value, which said adding-subtracting means adds or subtracts when the determination of said reply delay monitoring means or receiving interval monitoring means is a communication error, is a third variation value, being a value different from said second variation value; and further said third variation value is a value smaller than a permitted accumulation value, being a difference between said abnormal-side limit value and normal-side limit value.

10. (currently amended): The electronic control unit according to claim 8, wherein said first control circuit section comprises a reply-waiting data table;
wherein said reply-waiting data table ~~aets-operates~~ as a transmission-side command memory arranged so as to sequentially save a transmission command, which said first control circuit section has transmitted to said second control circuit section, and to erase said saved command when said first control circuit section has received a confirmation reply data from said second control circuit section; and
wherein said reply delay monitoring means ~~aets-operates~~ as reply error determination means for making an error determination when a save time period of a-leading data remained in said transmission-side command memory exceeds a predetermined value, and a command determined as a reply error and wherein a command having a confirmation reply of any receiving failure are sequentially deleted from said transmission-side command memory, and stored anew in the transmission-side command memory at the time of being transmitted again.

11. (currently amended): The electronic control unit according to ~~claims-claim~~ claim 8, wherein said first control circuit section comprises a first set data memory; and
wherein said first set data memory acts as a data memory in which stored is a part or all of various control constants such as first variation value, second variation value, normal-side limit value, abnormal-side limit value, or initial value to be processed in said first adding-subtracting means; or a part or all of various control constants such as permitted values of a reply

response time period or a receiving interval time period to be used in said first communication error determination means; and

wherein a part or all of said various control constants are transferred and written from a non-volatile program memory cooperating with said microprocessor.

12. (currently amended): The electronic control unit according to claims 8, wherein said second control circuit section comprises a second set data memory; ~~and,~~
wherein said second set data memory ~~acts-operates~~ as a data memory in which ~~stored is a~~ part or all of various control constants such as first variation value, second variation value, normal-side limit value, abnormal-side limit value, or initial value to be processed in said second adding-subtracting means are stored; or wherein a part or all of various control constants such as permitted value of a receiving interval time period to be used in said second communication error determination means are stored; and
wherein a part or all of said various control constants are transmitted and written from a non-volatile program memory cooperating with said microprocessor via said first and second series-parallel converters.

13. (currently amended): The electronic control unit according to claims 6, wherein said second control circuit section comprises current value report means;

wherein said current value report means ~~aets-operates~~ as means for adding a current value of said second adding-subtracting means to said status information, and regularly reporting a ~~resulting-result~~ information to said first control circuit section.

14. (currently amended): The electronic control unit according to claims 6, wherein said first control circuit section comprises a direct input/output signal interface circuit, and either said first or second control circuit section comprises a watchdog timer and error occurrence storage means;

wherein said direct input/output signal interface circuit is bus-connected to said microprocessor;

wherein said microprocessor is arranged so as to generate an output signal in response to a direct input signal having been inputted via said direct input signal interface, an indirect input signal having been received by serial communication from a second series-parallel converter provided in said second control circuit section, and a content of said program memory to drive an electrical load group, which is connected to said direct output signal interface circuit, and to transmit an indirect output signal via said first and second series-parallel converters to the second control circuit section;

wherein said watchdog timer ~~aets-operates~~ as a run-away monitoring timer circuit that monitors a watchdog clear signal, being a pulse train, which said microprocessor generates, and generates a reset pulse signal when a pulse width of said watchdog clear signal exceeds a predetermined value;

wherein said error occurrence storage means ~~acts-operates~~ as an error storage circuit that stores said first and second error detection signals or a reset pulse signal to bring annunciation means such as alarm, display, printing, and history save in operation when said error detection signals are generated, and when the reset pulse signal provided by said watchdog timer is generated; and

wherein said microprocessor is initialized and restarted when said watchdog timer generates a reset pulse signal and when said second error detection signal is generated, and a communication control circuit section of said second control circuit section is initialized and restarted when said watchdog timer generates a reset pulse signal and when said first error detection signal is generated.

15. (currently amended): The electronic control unit according to claim 14, wherein said second control circuit section comprises an auxiliary CPU, and said first control circuit section comprises run-away monitoring means with respect to said auxiliary CPU;

wherein said auxiliary CPU ~~acts-operates~~ as a microprocessor that is contained in said second control circuit section along with an auxiliary program memory cooperating with said auxiliary CPU, an operation processing auxiliary RAM memory, an indirect input/output signal interface circuit and a second series-parallel converter, transmits an indirect input signal associated with a signal having been inputted via said indirect input signal interface circuit to the first control circuit section via said first and second series-parallel converters, and drives an electrical load group that are connected to said indirect output signal interface circuit with an

output associated with an indirect output signal having been received from said first control circuit section via said first and second series-parallel converters;

wherein said run-away monitoring means ~~aets-operates~~ as means for monitoring with said microprocessor a watchdog clear signal, being a pulse train that said auxiliary CPU generates, and generating a reset pulse signal when a pulse width of said watchdog clear signal exceeds a predetermined value; and

wherein when said run-away monitoring means generates a reset pulse signal, when said watchdog timer generates a reset pulse signal and when said first error detection signal is generated, said auxiliary CPU is initialized and restarted, and said error storage circuit is arranged to store the occurrence of error.

16. (currently amended): The electronic control unit according to claim 14, wherein said error occurrence storage means is constituted of a count storage circuit; ~~and,~~

wherein said count storage circuit counts an OR output with respect to said first and second error detection signals and a reset pulse signal provided by the watchdog timer or the run-away monitoring means, and brings said annunciation means in operation when said count value reaches a predetermined value.

17. (currently amended): The electronic control unit according to claim 14, wherein at least one of said first and second control circuit sections comprises driving stop means and clear means;

wherein said driving stop means ~~aets-operates~~ as a gate circuit that operates when said error occurrence storage means stores an error occurrence to inhibit driving of specified electrical loads, being a part of said electrical load group₁, and

wherein said clear means ~~aets-operates~~ as means for initializing an error storage signal provided by said error occurrence storage means by manual operation such as turning on a power supply switch again.

18. (currently amended): The electronic control unit according to claim 16, wherein at least one of said first and second control circuit sections comprises driving stop means and clear means₁,

wherein said driving stop means ~~aets-operates~~ as a gate circuit that operates when a count value of said count storage circuit is not less than a predetermined value to inhibit driving of specified electrical loads, being a part of said electrical load group₁, and

wherein said clear means ~~aets-operates~~ as means for initializing a current value of said count storage circuit by manual operation such as turning on a power supply switch again.